Q.P. Code: 18EC0402 **R18**

Reg. No: | | | | | | | | | | |

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY:: PUTTUR

(AUTONOMOUS)

B.Tech II Year I Semester Supplementary Examinations Feb-2021

DIGITAL SYSTEM DESIGN

(Electronics & Communication Engineering)

Time: 3 hours Max. Marks: 60

PART-A

(Answer all the Questions **5 x 2 = 10** Marks)

1	a	Show that (X + Y' + XY)(X + Y')(X'Y) = 0.	2M
	b	Find the minterms of the given Boolean expressions. F=C_1D+AB C_1+ABD_1+A_1B_1D.	2M
	c	Draw the circuit of ring counter.	2M
	d	What are the advantages of PLDs.	2M
	e	Write a VHDL Program for 1x4 DEMUX in Dataflow Model.	2M

PART-B

(Answer all Five Units 5 x 10 = 50 Marks)

UNIT-I

2	a	Convert the following to binary and then to gray code i) $(1111)_{16}$ ii) $(BC54)_{16}$ iii) $(237)_8$ iv) $(164)_{10}$ v) $(323)_8$	5M
	b	State and prove De Morgan's theorem.	5M
		OR	
3	a	Express the Boolean function F= A+B'C as a sum of minterms.	5M
	b	Obtain the Dual and complement to the following Boolean expressions i) F=AB+A (B+C) + B' (B+D) ii) F=A'B+A'BC'+A'BCD+A'BC'D'E	5M

UNIT-II

4	a	Write the design procedure for combinational circuit.	5M
	b	Simplify F(A,B,C,D) = Σ (4,5,6,7,12,13,14) +d(1,9,11,15) using K-map.	5M
		OR	
5	a	Minimize the given Boolean function, F (A, B,C,D) = Σ m(0,1,2,3,6,7,13,15) using Tabulation method and implement it using basic gates.	5M
	b	Design & implement the Full Adder.	5M

UNIT-III

6	a	What is the need for Master Slave JK FF and explain its operation with neat diagrams.	5M
	b	Design and implement a 2 bit Up-Down Counter using JK FF's.	5M
		OR	
7	a	Draw the logic diagram of a JK – flip flop and explain its operation.	6M
	b	Explain the operation of Pseudo Random Binary Sequence Generator with a neat diagram.	4M

UNIT-IV

8	a	Briefly introduce the content addressable memory.	6M
	b	Implement the following functions using a PLA f1(w,x,y)=Σm(3,5,6,7).	4M
		OR	
9	a	Explain the architecture of PLA.	5M
	b	Generate the following Boolean function using PAL with 4 inputs and 4 outputs i)Y3= a'bc'd+a'bcd'+abc'd (ii)Y2=a'bcd'+a'bcd+abcd	5M

UNIT-V

10	a	Explain in detail different modeling styles of VHDL with suitable examples.	5M
	b	Write a VHDL program for Full adder.	5M

OR

11	a	Explain the structure of a VHDL program.	5M
	b	Draw and explain in detail the VHDL design flow.	5M

END